REMARKS

Claims 1, 2, 4 through 15 and 17 through 23 are pending in this application. Claims 1, 7, and 15 are the independent claims.

Applicants would like to thank the Examiner for the courtesies extended to Applicants' representative in a telephone interview on May 4, 2004. Pursuant to MPEP §713.04, Applicants are concurrently submitting herewith an interview summary of the aforementioned telephone interview.

Claims 1, 2, 4 through 15 and 17 through 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992. Applicants respectfully traverse the rejection and request reconsideration thereof for the following reasons.

35 U.S.C. § 102(b) Rejections

Claims 1 through 2, 4 through 15 and 17 through 23 are Patentable Over the Prior Art

Claims 1 through 2, 4 through 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992. Applicants respectfully traverse the rejection.

Referring to claim 1, the Examiner states that Killian et al. has taught a processor comprising:

"(a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.

(b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:

(i) means for truncating generated address references of the second bit size to the first bit size. See column 10, line 62, to column 11, line 5. In this passage, Killian has explained that the 32-bit architecture ignores overflow (i.e., performs truncation) during addition operations. Since Killian's system is backward compatible with the aforementioned 32-bit architecture, it follows that Killian's system would perform the same operations as the 32-bit architecture. Therefore, in overflow situations, truncation would be performed on 64-bit data (since the data path and register size of Killian's system is 64-bits) in order to obtain 32-bit data.

(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references. See column

12, lines 45-65. Note that 32-bit data is sign extended for use in the extended architecture. However, it should also be realized from column 3, line 67, to column 4, line 10, that when timing constraints militate against sign-extension, the address will be zero-extended instead, using zeroing circuitry. In fact, this zeroing circuitry is invoked when the system is in m-bit user mode (32-bit user mode). When the system is in other modes, sign-extension will occur. From the very top of Fig. 5E of Killian, it can be seen that a "32-bit user mode" signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended.

Claim 1 recites, *inter alia*:

"means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references."

As a result, claim 1 clearly recites that the "address format control signal" is to be used to both indicate when to zero-extend and when to sign-extend the address references. Contrary to the Examiner's assertion, Killian et al. does not disclose or suggest "means for extending to the second bit size the truncated generated address references based at least in part on a setting of **an address format control signal**, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of **the address format control signal** to indicate sign-extension of the truncated generated address references," as recited in claim 1. (Emphasis added.) Killian et al. fails to disclose or suggest an equivalent structure to the above extending means using the value of a **single signal** to indicate whether to zero-extend or sign-extend the truncated generated address references. Instead, Killian et al. uses separate "sign-extension hardware" and "zeroing circuitry" to sign-extend and zero-extend, respectively, the output addresses. In addition, the sign-extension hardware and the zeroing circuitry operate independently. (Column 3, line 67 to claim 4, line 10.) In other words, **no single signal (e.g., the address format control signal**, as recited in claim 1) indicates to the sign-extension hardware to sign-extend on one value and to the zeroing circuitry to zero-extend on another value of the signal. In addition, the zeroing circuitry only operates to force the (N-m) most significant bits to zero when the m-bit user mode

signal exists. Thus, the zeroing circuitry is only operating on the (N-m) most significant bits and not the "truncated generated address references," recited in claim 1. Similarly, when the zeroing circuitry allows the (N-m) most significant bits to pass unchanged, the zeroing circuitry is not operating to "indicate sign-extension of the truncated generated address references," as recited in claim 1, since the passed address is not "truncated" nor is it sign-extended as a result of the m-bit user mode signal being cleared – it already is sign-extended. Therefore, there is no equivalent **single signal** in Killian et al. that is used to explicitly specify whether to zero-extend or sign-extend the truncated generated addresses. As such, the Examiner has failed to establish a *prima facie* case of anticipation of claim 1, since Killian et al. fails to disclose each and every element of claim 1. Accordingly, the Section 102 rejection of claim 1 is believed to be overcome and Applicants respectfully request the Section 102 rejection of claim 1, and the claims that depend therefrom, be withdrawn.

Claims 7 and 15 were amended during prosecution of the parent application to contain similar recitations as claim 1. Therefore, for at least those reasons given above for claim 1, Applicants also believe that the Examiner has failed to establish a *prima facie* case of anticipation of claims 7 and 15 and, therefore, the Section 102 rejection of claims 7 and 15, and of the claims that depend variously therefrom, has been overcome. Accordingly, Applicants respectfully request the Section 102 rejection of claims 7 and 15, and of the claims that depend, respectively, therefrom be withdrawn.

Therefore, Applicants believe all currently pending claims to be allowable and respectfully request a notice of allowance to that effect be issued.

CONCLUSION

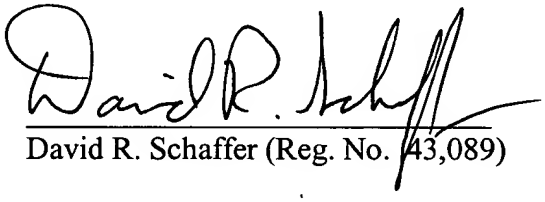
In view of the above remarks, Applicants respectfully submit that the present case is in condition for allowance and again request that the Examiner issue a notice of allowance to that effect for all currently pending claims.

Applicants authorize the Commissioner to charge any fees determined to be due under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4263 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON



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David R. Schaffer (Reg. No. 43,089)

1500 K Street, N.W.
Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
Fax: (202) 220-4201

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